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DESIGN OF VOLTAGE-MODE INSTRUMENTATION AMPLIFIERS FOR ECG SIGNALS USING CMOS TECHNOLOGY

Frederick Ray I. Gomez*, Sherwin Paul Almazan, Lendl Israel Alunan, John Martin Jarillas, Maria Theresa De Leon, Marc Rosales

* New Product Introduction Department, Back-End Manufacturing & Technology, STMicroelectronics, Inc. 9 Mountain Drive, Light Industry & Science Park II, Brgy. La Mesa, Calamba City, Laguna, Philippines 4027

Microelectronics and Microprocessors Laboratory, Electrical and Electronics Engineering Institute University of the Philippines, Diliman, Quezon City, Philippines 1101

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ABSTRACT

Design and implementation of four monolithic voltage-mode instrumentation amplifier (in-amp) topologies are studied and discussed in this paper. These in-amp topologies utilize op-amps with rail-to-rail input and output stages. As recommended in [1], the operational amplifier (op-amp) implementation used in this study employs a complementary differential pair with n-type metal-oxide semiconductor (NMOS) cascode load input stage and a push-pull inverter output stage. The op-amp is designed to achieve the highest possible common-mode rejection ratio (CMRR) while maintaining stability. A compensation network is also designed to maintain stability when the designed op-amp is incorporated into the in-amp. The four voltage-mode in-amp topologies are designed for handling biomedical signals specifically that of the Electrocardiogram (ECG), and are implemented in a 0.25µm Complementary Metal-Oxide Semiconductor (CMOS) process. Simulations achieved a CMRR of about 90 dB for all topologies, with the 2-op-amp in-amp showing an advantage over its 3-op-amp counterparts in terms of power consumption. The simulations are obtained for a gain of 200 and power supply of 2.5V.

INTRODUCTION

The measurement of low-energy bio-potential signals such as the Electrocardiogram (ECG) makes the in-amp a significant signal-conditioning block for biomedical systems. With the use of instrumentation amplifiers (in-amps), it is possible to accurately amplify these weak electric body signals even in the presence of high-amplitude common-mode noise and interference from other potential sources that may tend to corrupt the desired signal.

Having this critical application, in-amps are particularly designed to achieve high common-mode rejection ratio (CMRR) to correctly extract and amplify low-amplitude differential signals that contain the information, and to block unwanted noise potentials that are usually common to the in-amp inputs [2].

Traditionally, in-amps are realized using voltage-mode configurations, which include the most conventional in-amp implementation, the 3-op-amp in-amp. These topologies are formed using operational amplifiers (op-amps) and resistor networks. To achieve high CMRR, the resistors to be used for the voltage-mode in-amps should be precisely matched and thus, demands the expensive laser trimming technology for high resistor accuracy [3].

The implemented voltage-mode in-amp topologies are: (1) subtractor, (2) subtractor with input buffers, (3) 3-op-amp, and (4) 2-op-amp, which are designed and implemented using 0.25µm Complementary Metal-Oxide Semiconductor (CMOS) technology. These in-amp circuits are designed to achieve target specifications comparable with that of commercially-available in-amps. The parameters used in characterizing the performance of the in-amps include CMRR, input and output impedance, input and output swing, supply current and power consumption. A simulated ECG signal with common-mode noise is used in the testing and simulation of these different in-amp circuits to determine the best in-amp configuration for ECG signals.

RAİL-TO-RAİL OPERATİONAL AMPLİFİER

The op-amp topology used in all the in-amp circuits, shown in Fig. 1, employs the complementary differential pair with cascode load in its input stage because it has fewer stages and is stable even without compensation.

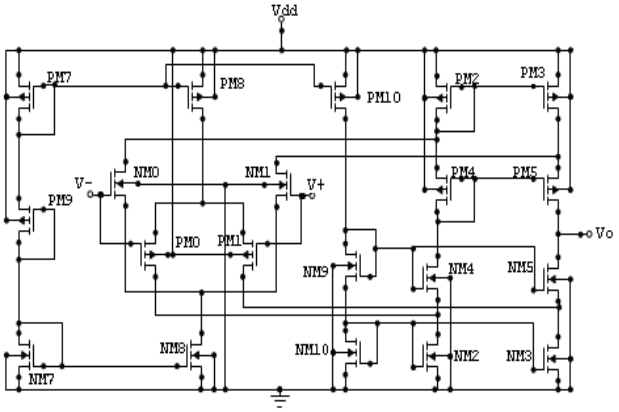

Figure 1. Complementary differential pair with NMOS cascode load.

Simulations have proven that performance is the same even if the cascode load is NMOS (n-type metal-oxide semiconductor) or PMOS (p-type metal-oxide semiconductor), so the NMOS load was chosen because NMOS transistors are naturally smaller than their PMOS counterparts, given the same drain current, thus resulting in reduced die area [1].

The chosen output stage is the push-pull inverter shown in Fig. 2 because it enables higher gain and output voltage swing range. In addition, its operating point is easily adjusted to match the rail-to-rail input stage.

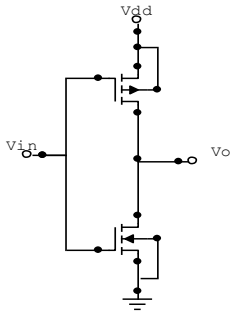

Figure 2. Push-pull inverter output stage.

Instead of using the minimum length of 0.25µm, all the transistor lengths were set to 1.2µm in order to minimize the short channel effects, which become significant at channel lengths of less than 1µm. The initial widths are determined using the drain current equation for a MOSFET in the saturation region, given in (1). Furthermore, submicron lengths for differential input pairs tend to introduce large offset voltage [2], [4]. The tail current is set to 20uA, to minimize the total supply current and to meet the limits on power consumption. The constants used in the following equations are derived from simulations.

$$I_D = \frac{k'}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2 \qquad (1)$$

$$V_{OV} = \frac{2I_{DS}}{g_M} = V_{GS} - V_T = 0.16V \qquad (2)$$

$$W_N = \frac{2LI_D}{k'_N(V_{GS}-V_T)^2} = \frac{(2)(1.2\mu m)(20\mu A)}{(205\mu A/V^2)(0.16V)^2} = 9.146\mu m \quad (3)$$

$$W_P = \frac{2LI_D}{k'_P(V_{GS}-V_T)^2} = \frac{(2)(1.2\mu m)(20\mu A)}{(48.1\mu A/V^2)(0.16V)^2} = 38.98\mu m \quad (4)$$

The widths for the NMOS and PMOS are rounded-off to 10µm and 40µm respectively. For an Ibias/2 current, a width of 5µm and 20µm is used for NMOS and PMOS transistors, respectively. Plugging these values into the schematic produced a differential-mode voltage gain of less than 10K, which is below the target gain of at least 1M. The transistor widths are then resized to increase the gain. A series of simulations aimed at characterizing the voltage-mode in-amp are then carried out. The effects of varying the width of each transistor on the in-amp parameters such as common-mode gain, 3-dB bandwidth, unity-gain bandwidth and phase margin are obtained and analyzed.

To facilitate in the layout implementation, sizes that are multiples of each other were chosen. Initial simulations showed that the subtractor with input buffers alone showed signs of instability. For this reason, the op-amp was designed to increase the phase margin for all the in-amp configurations. The stability of the subtractor with input buffers is severely degraded when the width of the biasing transistor NM10 is increased from 5µm to 6µm, based on additional simulations. For this scenario, multiples of 6 were chosen for the channel lengths. However, since 6µm is the nearest even multiple-of-6 for transistor NM10's width, it becomes necessary to use this size, which gives an unstable output. To resolve this issue, most of the other transistor sizes were decreased, thereby improving the op-amp's over-all frequency response.

For the 3-op-amp in-amp, on the other hand, decreasing the widths of the input differential pair decreases the transconductance, increases the gain, and in turn decreases the unity-gain bandwidth. Inferring from the observed trends, the final sizes for the op-amp transistors were achieved.

The results of the op-amp design are presented in Table 1. It contains parameters obtained from the layout implementation. Parasitic capacitances and resistances are extracted after completing the layout implementation to predict the circuit's behavior more accurately. As can be seen from Table I, the target differential gain of at least 1M is achieved while having acceptable values for the other parameters.

Table 1. Op-amp parameters.

Parameters	Op-Amp Layout Values
A_{DM}	1.8706M
A_{CM}	33.4579m
CMRR	150.9496dB
OVSR	9.7527µV to 2.5V
ICMRR	2.82mV to 2.49V
Input Offset Voltage	33.7289µV
Supply Current	275.9672µA
Power Consumption	689.9181µW
R_{IN}^+	11.9538GΩ
R_{IN}^-	181.5438MΩ
R_{OUT}	82.3676KΩ
Phase Margin	94 deg
3-dB BW	30.3144Hz
PSRR @ 60Hz	94.6480dB
Settling Time	553.51920ns
Slew Rate	25.3924V/µs

VOLTAGE-MODE INSTRUMENTATION AMPLIFIERS

The target parameters for the voltage mode in-amps are set to be comparable to the specifications of commercially available in-amps, as shown in Table 2.

Table 2. Voltage-mode in-amp design constraints.

Parameters	Values
Differential –Mode Gain	200
Common-Mode Rejection	≥ 90dB
Input and Output Swing	Rail-to-Rail
Input Impedance	≥ 100 KΩ
Supply Voltage	2.5V
Supply Current	≤ 2mA
Power Consumption	≤ 5mW

All four voltage-mode in-amp circuits are implemented using the same op-amp with uniform sizing, biasing and compensation, to ensure a reasonable and justifiable comparison of the different voltage-mode architectures. The op-amp discussed in the previous section is used in all the voltage-mode in-amp implementations, making the input common-mode range and output voltage swing of the in-amps achieve a rail-to-rail operation. The target CMRR is at least 90dB to effectively design the in-amps for critical applications, such as biomedical instrumentation.

It was observed from simulations that increasing the absolute value of the gain-setting resistors significantly improves the CMRR of the in-amp. However, resistors occupy a huge amount of area in the actual layout. Thus, the highest resistance value to be used in all designs was limited to 50K because of area constraints.

The simplest way of implementing an in-amp is by using a single op-amp configured as a differential amplifier, commonly known as the subtractor [3], as shown in Fig. 3. However, the unequal impedances at the two input terminals also produce different input currents to flow, depending on which input receives the applied voltage. This imbalance in the sources' resistance will degrade the in-amp's CMRR [5].

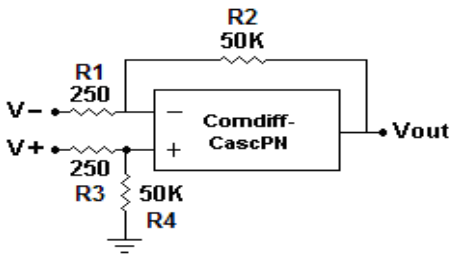

Figure 3. Subtractor schematic diagram.

The topology in Fig. 4 provides the same differential gain as the subtractor. However, the input impedance is improved. This is due to the addition of two op-amps configured as voltage followers, thereby providing the high input impedance necessary to avoid loading down the input source.

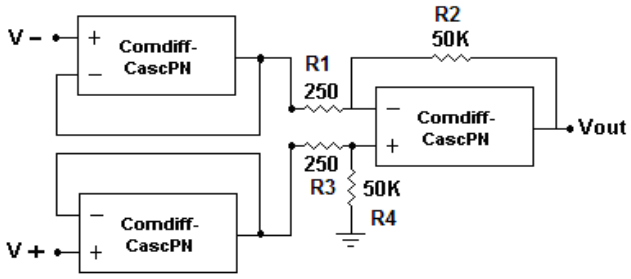

Figure 4. Subtractor with input buffers schematic design.

Two op-amps with a non-inverting voltage amplifier configuration form the input or first stage of the 3-op-amp in-amp illustrated in Fig. 5, and their output terminals are connected to the input of the subtractor. This topology is a further improvement to the subtractor with input buffers, since the input stage provides an additional gain for the in-amp.

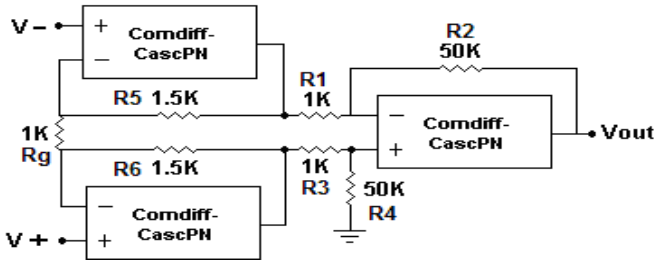

Figure 5. 3-op-amp in-amp schematic design.

The 2-op-amp in-amp topology shown in Fig. 6 has the evident advantage of requiring only two op-amps, rather than the 3-op-amp in-amp as discussed in the preceding sections, and thus a decrease in cost and power consumption [3] [6].

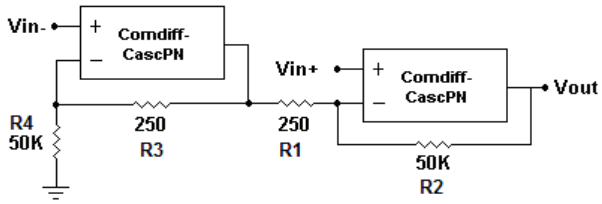

Figure 6. 2-op-amp in-amp schematic design.

REPRESENTATION OF THE ECG SIGNALS

To verify the capability of the implemented in-amps to accurately amplify low-amplitude ECG signals in the presence of high-energy common-mode noise, a representation of an ECG waveform is employed. A piece-wise linear voltage source file is specifically used for this purpose.

The model used in plotting the signal is adapted from related literature on biomedical signals. In addition, the simulated ECG signal was made to last for only 3 periods, so that simulations would not take much time. The simulated ECG signal is then connected to the in-amp's input terminals.

To add common-mode noise to the ECG signal, a cascade of 100mV-sinusoids at 60, 120, 180 and 240Hz were introduced to the in-amp as input common-mode voltages. Shown in Fig.7 is the schematic diagram of the setup. A 1.25V DC voltage source was also used as a commode-mode input voltage to maintain the correct biasing of the in-amp.

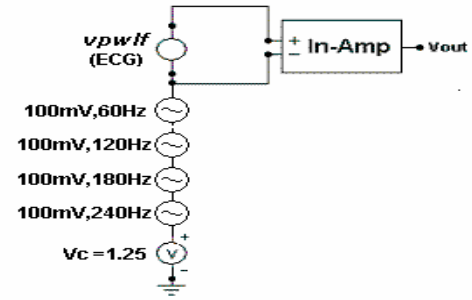

Figure 7. Set-up for the in-amp as it accepts ECG signal with common-mode noise as inputs.

RESULTS AND ANALYSES

The subtractor in-amp exhibits the basic in-amp function of rejecting common-mode voltage, with a CMRR above the 90 dB target for both schematic and layout implementations. However, this topology suffers from unmatched low impedances seen at the input terminals. This is due to the fact that the input impedance of the subtractor is dependent on the values of the resistors used in the resistor-feedback network, and is not affected by the inherent high input impedance of the op-amp. Nevertheless, having the least circuit components, the subtractor consumes the least power among the voltage-mode in-amps, with power consumption way below the target specs.

On the other hand, as its name implies, the subtractor with input buffers increased the input impedance of the simple subtractor, but at the expense of consuming greater power than the 2-op-amp. It also poses the problem of instability for certain transistor sizing and biasing.

Contrary to the expected results, the 3-op-amp (the most conventional in-amp configuration) is the topology that is the most difficult to implement. Preliminary sizing and biasing of the op-amp used in this configuration makes the 3-op-amp fail the stability and CMRR requirements. The 3-op-amp in-amp consists of more cascaded stages and thus, is more prone to instability. This issue of instability, meanwhile, is solved by using a larger compensation network, and by more tedious tweaking and redesigning of the op-amps' sizing and biasing.

At a single supply of 2.5V, the four voltage-mode topologies have fairly close CMRR performance. However, the 2-op-amp in-amp proves to be the best choice for an in-amp topology. Not only does it achieve the high CMRR and high input impedance necessary for medical-grade in-amps -- it also outclasses its two triple-op-amp in-amp counterparts in terms of power consumption and stability, while significantly improving the input impedance of the subtractor. Fig. 8 shows the output plot obtained when the simulated ECG signal and common-mode noise is applied onto the 2-op-amp in-amp.

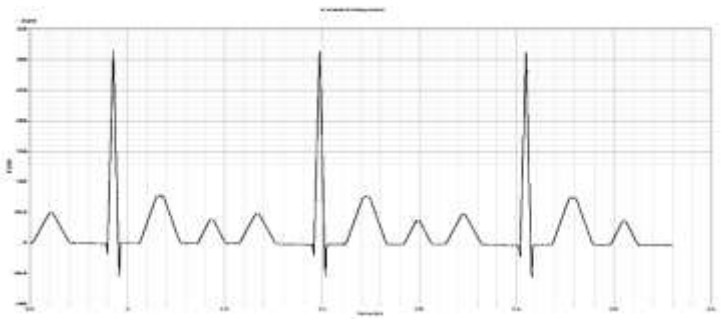

Figure 8. Transient analysis of 2-Op-Amp with ECG signal input and common-mode noise.

Summarized in Table 3 is the comparison between the achieved parameters of the 2-Op-Amp In-Amp and the specifications of the AD627 [7], which is also of the 2-op-amp configuration. This shows that the implemented in-amps can compete with the specifications of commercially-available in-amps.

Table 3. Parameters of 2-op-amp in-amp vs AD627

Parameters	2-Op-Amp In-Amp	AD627
A_{DM}	199.86	5 + 200k/Rg
A_{CM}	5.49m	7.062E-04
CMRR	91.23dB	77dB (G=5)
OVSR	21.35µV to 2.5V	Vss+25mV to +Vdd–70mV
Input Offset Voltage	-4.87mV	125µV
Supply Current	557.45µA	60µA
Power Consumption	1.39mW	Current*(±1.1 to ±18)
R_{IN}^{+}	1598.52GΩ	20G
R_{IN}^{-}	792.50GΩ	20G
R_{OUT}	7.02Ω	--
3-dB BW	257.49KHz	80KHz
PSRR @ 60Hz	104.47dB	100dB
Settling Time	577.45ns	135us
Slew Rate	24.37V/us	0.05V/us

CONCLUSIONS AND RECOMMENDATIONS

The paper investigated the use of the complementary differential pair with NMOS cascode load and push-pull inverter output stage op-amp as the building block for voltage-mode in-amps. However, as previously mentioned, stability becomes an issue when several op-amps are cascaded. Future implementations may investigate simpler op-amp architectures like the Miller op-amp, which has a lower gain but is more stable.

The trade-off between common-mode rejection and stability should always be taken into account in the design of in-amps. Simulations showed that as the common-mode gain of the in-amp decreases, CMRR increases but the stability is compromised. Cascading more stages to improve certain parameters such as CMRR worsens the stability of a system. This is evident in the implementation of the subtractor with input buffers and the 3-op-amp, which both have more stages and theoretically have higher CMRR, but are proven to be more unstable compared with other voltage-mode topologies..

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